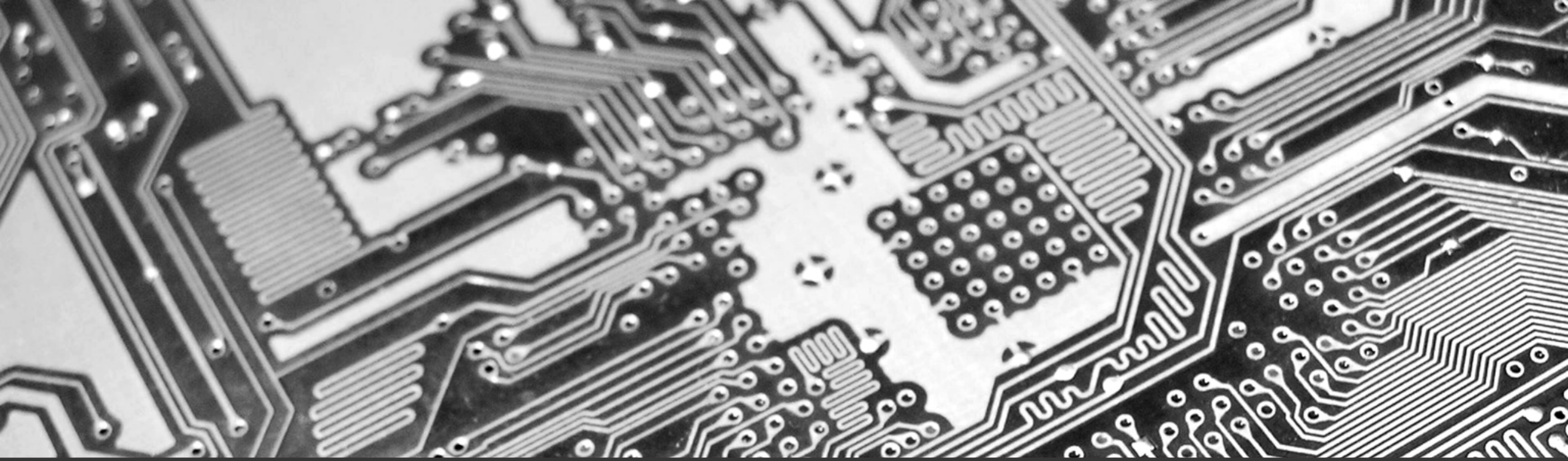

Field Programmable Gate Array (FPGA) for the Liquid Argon calorimeter back-end electronics in ATLAS

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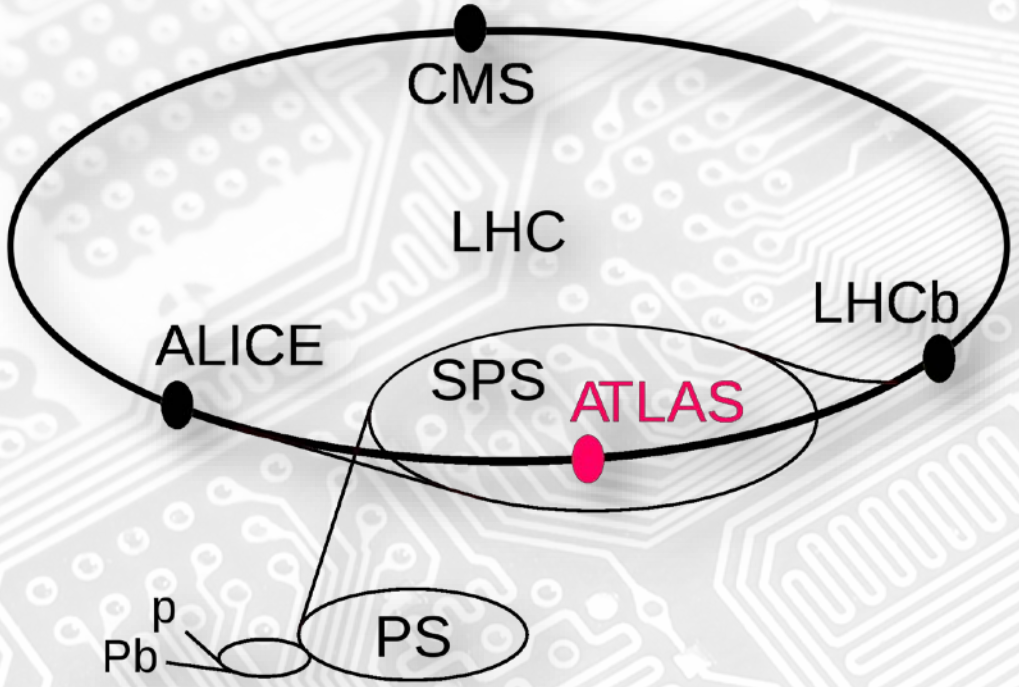
Università degli Studi di Milano

The ATLAS experiment at LHC

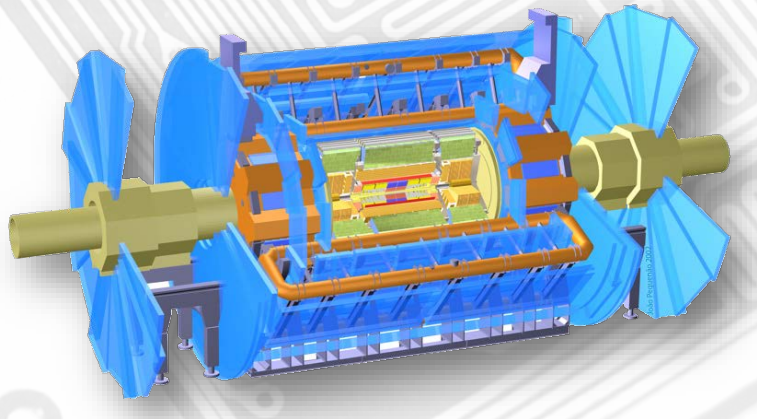
LHC stands for Large Hadron Collider:

- **Large** due to its size (approximately 27 km in circumference)
- **Hadron** because it accelerates protons (or ions)
- **Collider** because these particles form two beams travelling in opposite directions, which collide at four points where the two rings of the machine intersect.



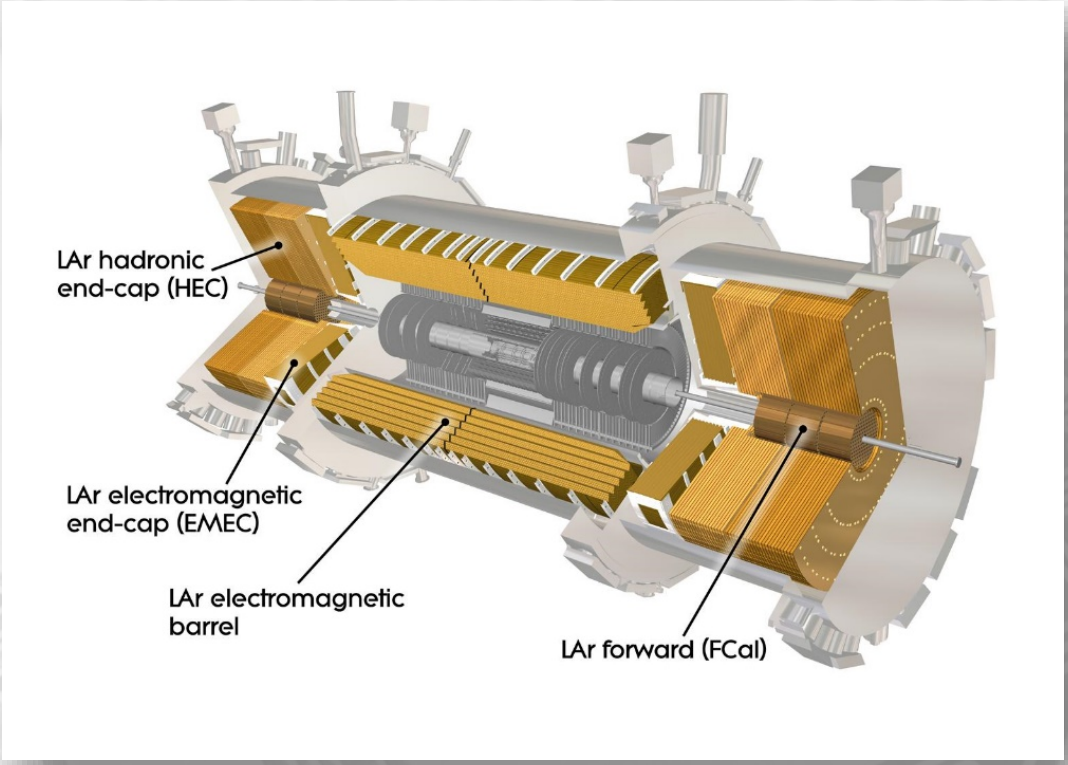
The **ATLAS detector** is located in one of these collision points and consists of four major components**:**

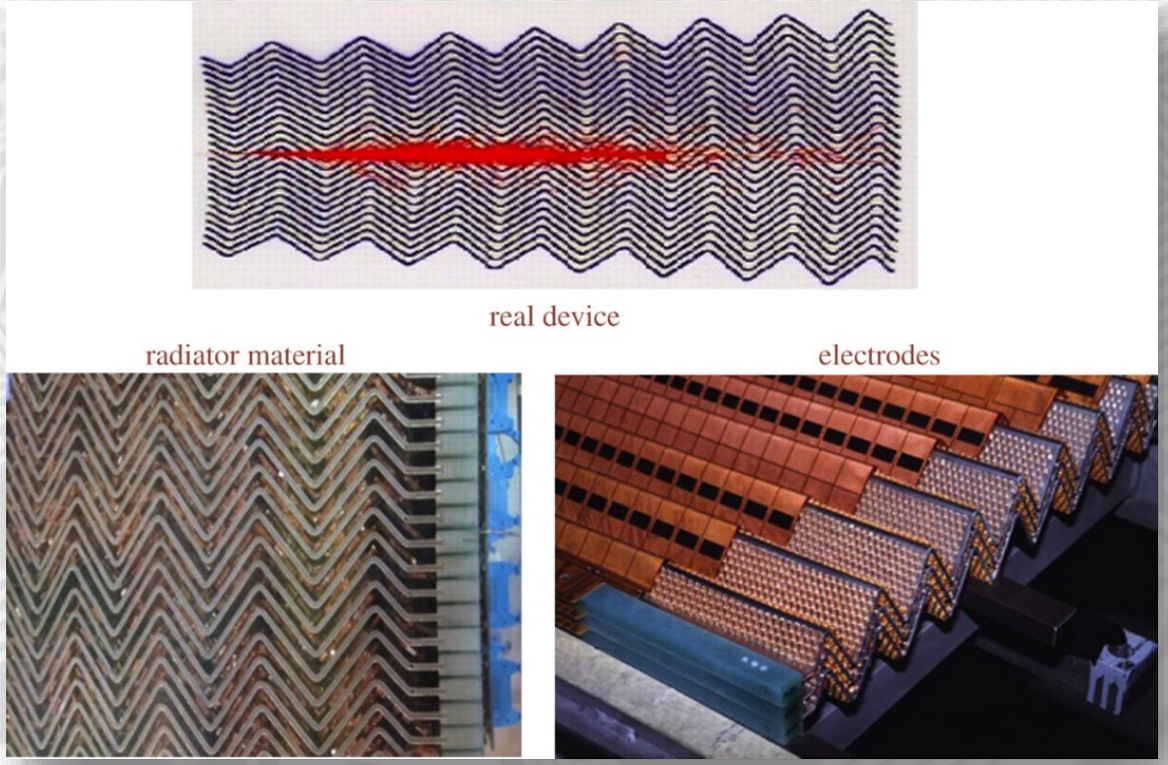
- **Inner detector**
  Measures the momentum and direction of charged particles
- **Calorimeters** (electromagnetic and hadronic)
  Measure the energies of electrons, photons and hadron jets
- **Muon spectrometer**
  Identifies and measures the momenta of muons
- **Magnet system** (solenoidal and toroidal)
  Bends charged particles for momentum measurements



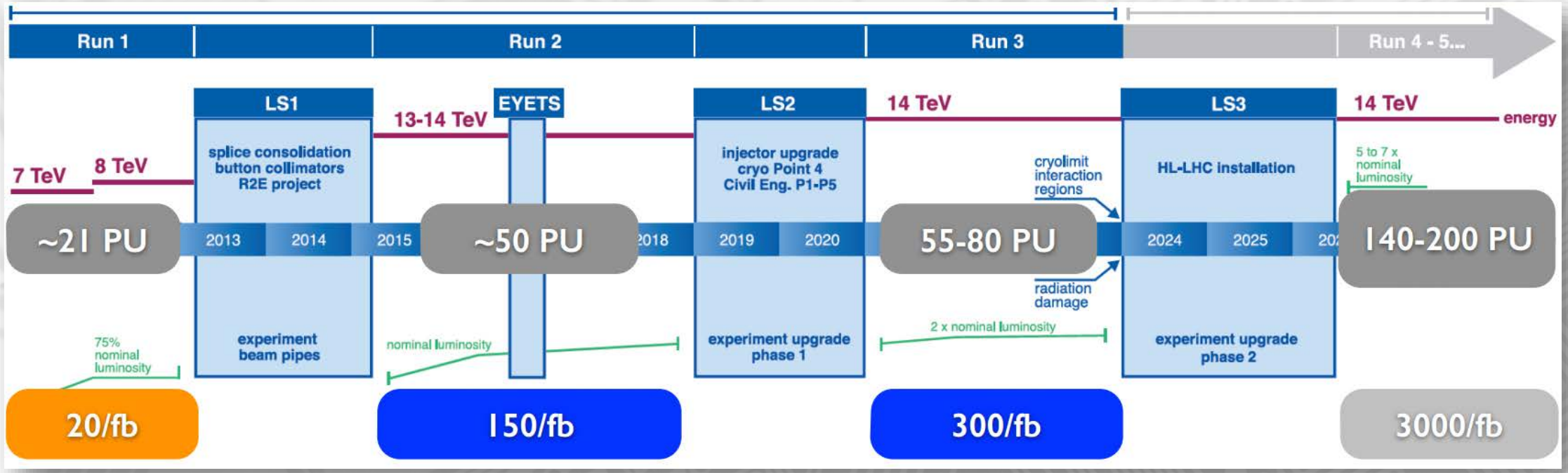
Liquid Argon (LAr) electromagnetic calorimeter

The **LAr calorimeter** is a sampling calorimeter with accordion-shaped lead absorbers and copper-kapton electrodes.
The electromagnetic calorimeter has been **successfully operated during LHC Run 1** (2009-2012) at 7 and 8 TeV energy and is now being operated during Run 2 which started in 2015 at a center of mass energy of 13 TeV.



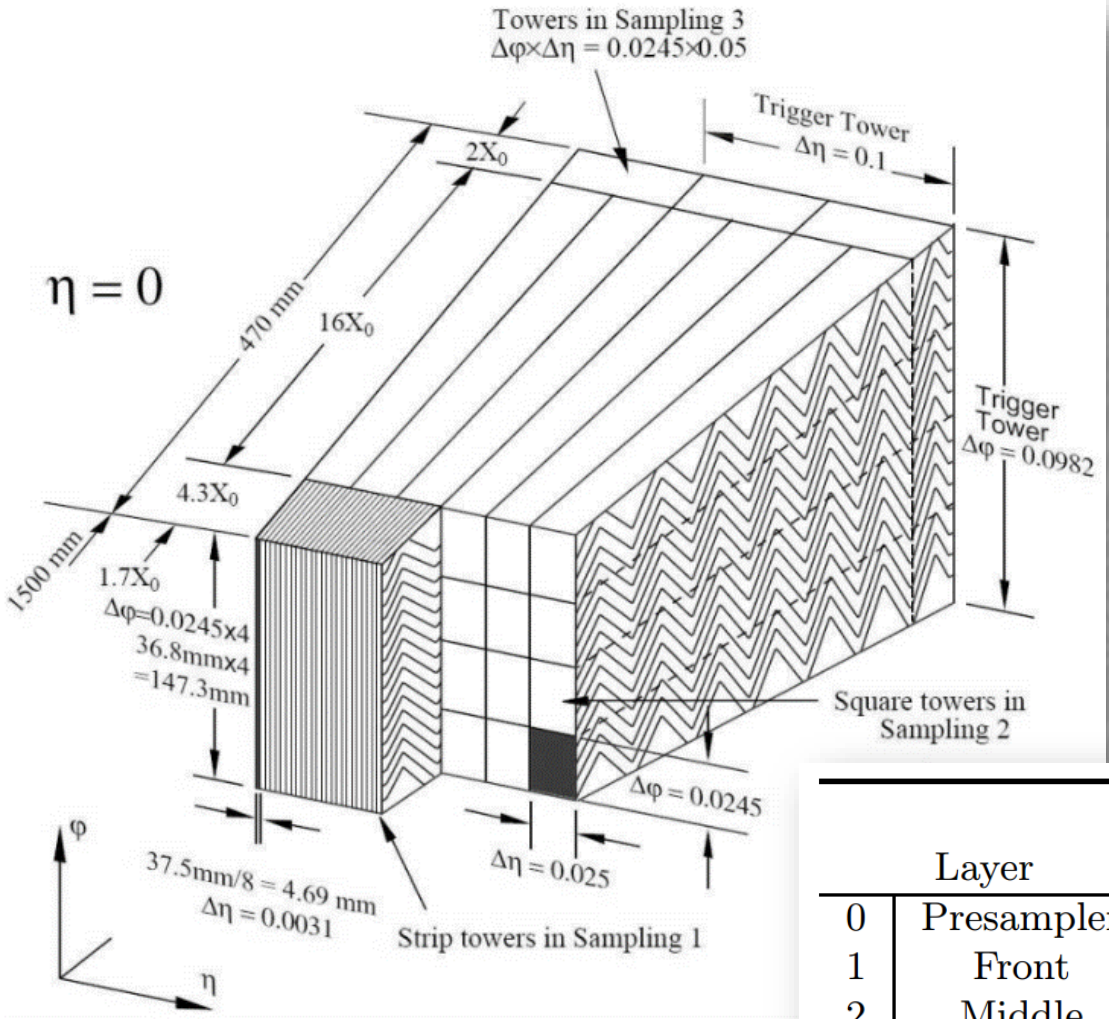


The Phase I upgrade



- **Phase I upgrade** will start in 2019
- An ultimate peak **instantaneous luminosity** of ~2.2×10^{34} cm^{-2} s^{-1} and an **integrated luminosity** of ~300 fb^{-1} are expected (for the Run 2 we expect an instantaneous luminosity of ~10^{34} cm^{-2} s^{-1} and an integrated luminosity of ~100 fb^{-1})
- **Event rate** (electrons and photons) selected by the calorimeter trigger will increase to 270 kHz with the present system, to be compared to a maximum Level 1 trigger bandwidth of 100 kHz
- The calorimeter bandwith must be brought back to the same level as in Run 2, about **20 kHz**.

Calorimeter Structure



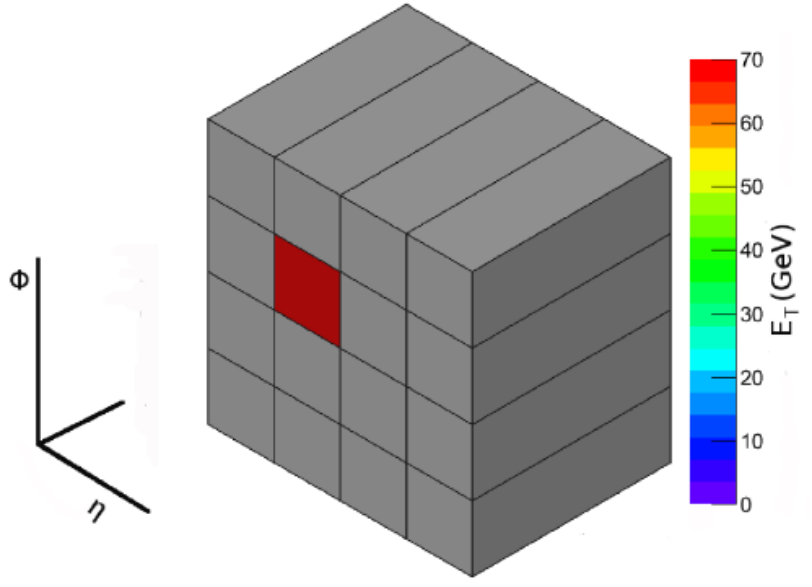
Structure for each layer:

- **Elementary Cells**
  Real calorimeter granularity
- **Tower**
  The existing trigger granularity
- **Super Cells**
  Phase I trigger granularity

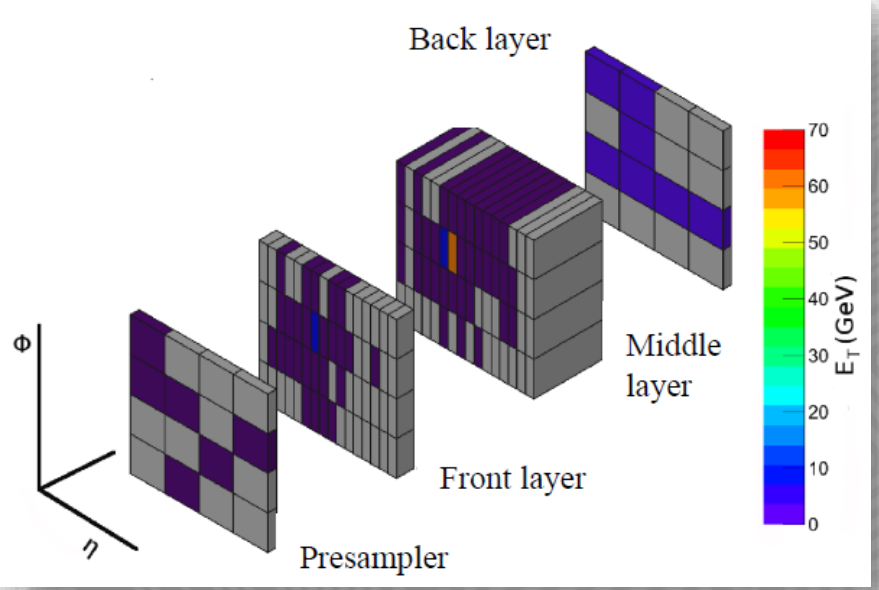
Layer		Elementary Cell	Trigger Tower		Super Cell	
		$\Delta\eta \times \Delta\phi$	$n_\eta \times n_\phi$	$\Delta\eta \times \Delta\phi$	$n_\eta \times n_\phi$	$\Delta\eta \times \Delta\phi$
0	Presampler	0.025×0.1	4×1	0.1×0.1	4×1	0.1×0.1
1	Front	0.003125×0.1	32×1		8×1	0.025×0.1
2	Middle	0.025×0.025	4×4		1×4	0.025×0.1
3	Back	0.05×0.025	2×4		2×4	0.1×0.1

Events from the calorimeter

Tower



Super Cells

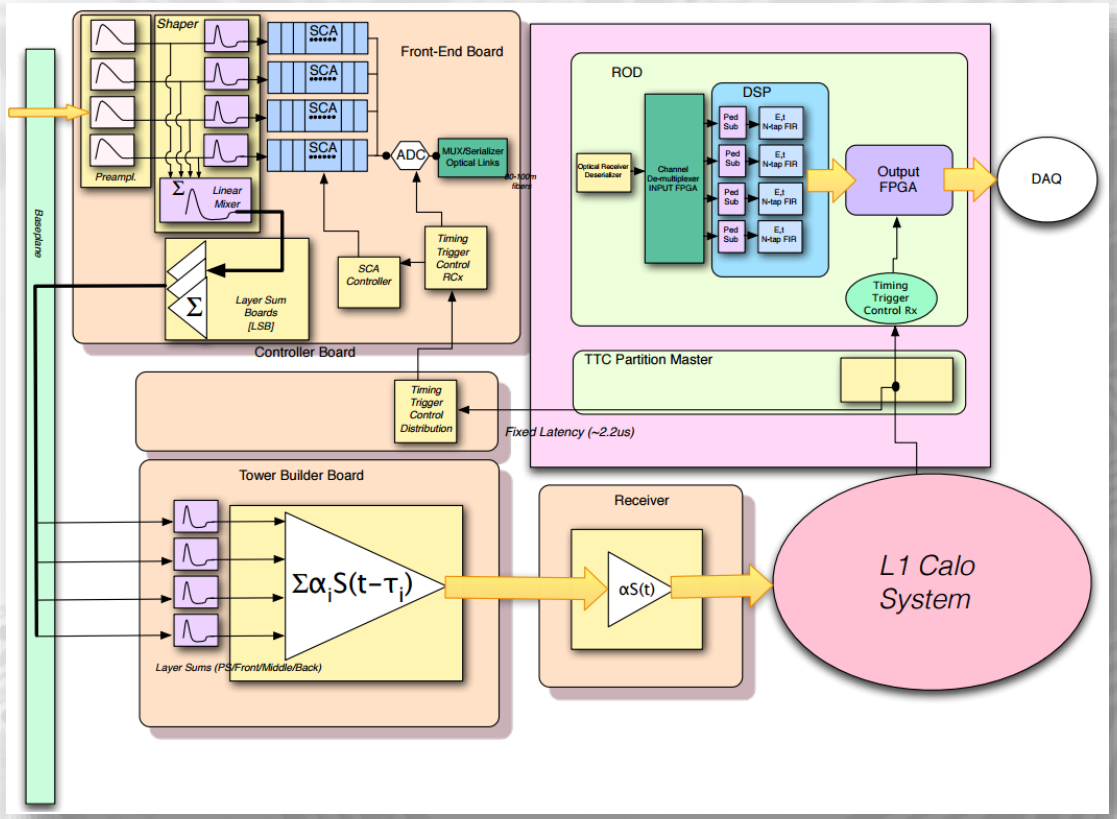


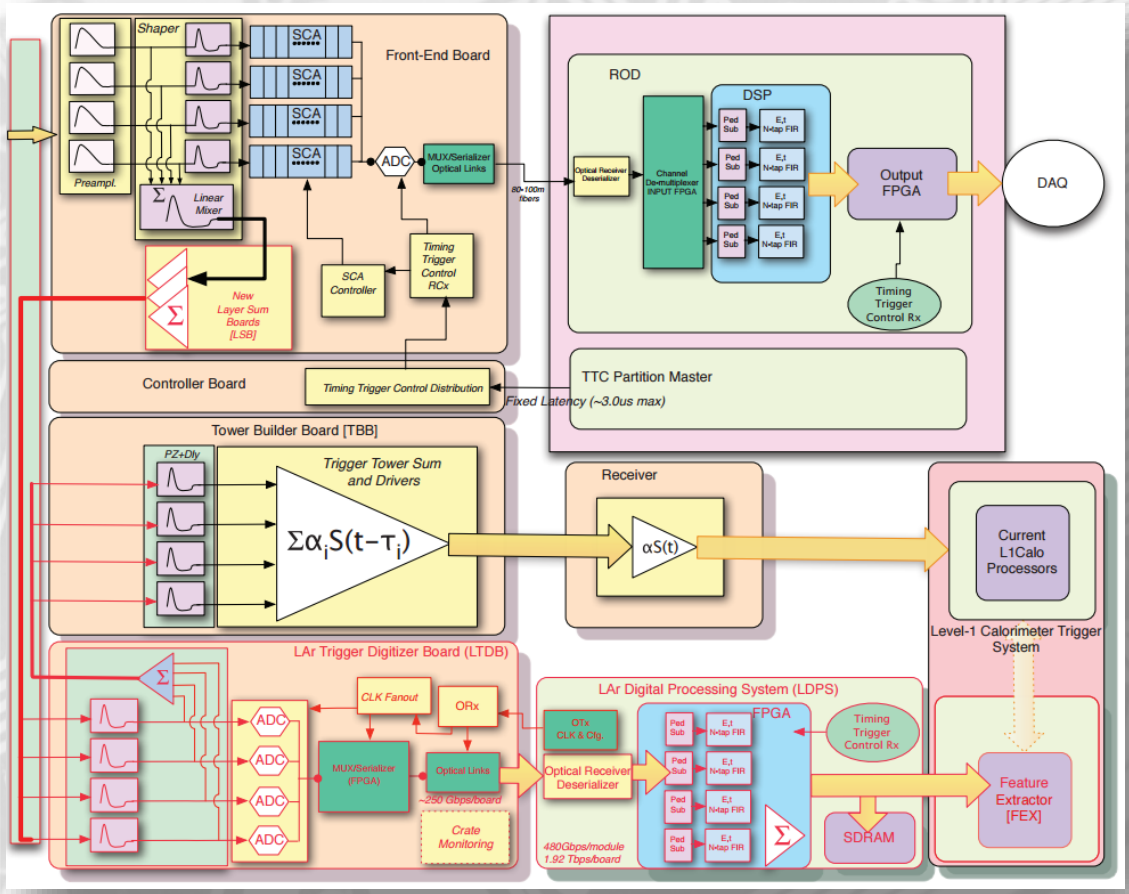
- **The existing calorimeter trigger information** is based on the concept of a *Trigger Tower* that sums the energy deposited across the longitudinal layers of the calorimeter
- **The new finer granularity** scheme is based on the so-called *Super Cells*, which provide information for each calorimeter layer for the full η range of the calorimeter
- With the *Super Cells* the **signal granularity will increase** by a factor 5-10

LAr trigger electronics upgrade

Comparison between the present and the phase I trigger electronics for LAr calorimeter:

- **New boards** (in red) to be installed in 2019
- **Summing** signals to obtain the Super Cells information
- **Digitization** of the calorimeter signals

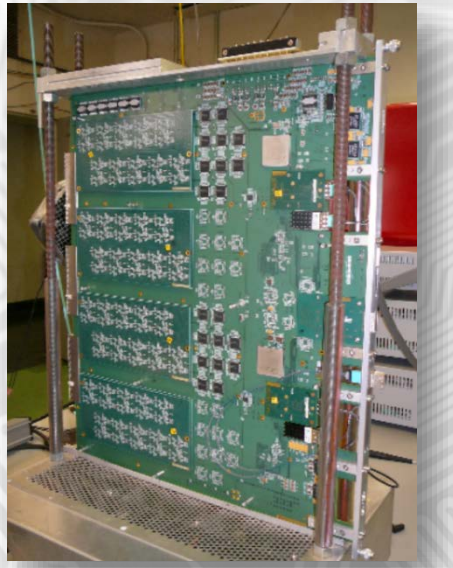




Demonstrators

LAr Trigger Digitizer Board (LTDB) demonstrator

- Handles up to 320 Super Cell signals
- Super Cell signals are digitized with 12 bit ADC@ 40MHz
- Multiplexing of 8 Super Cells on one 4.8 Gbit/s optical link
- 40 transmitter optical links
- Output : ~200Gbit/s per LTDB

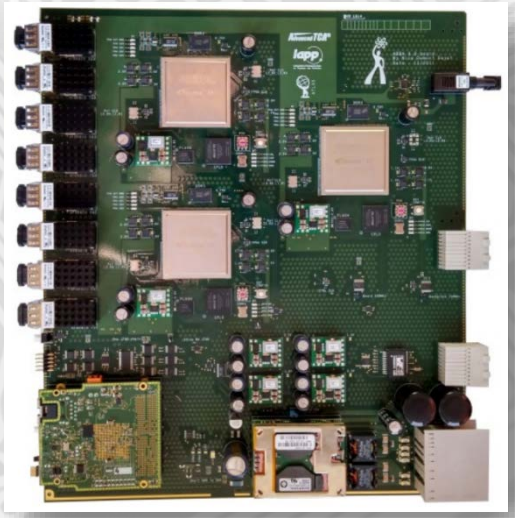


LAr Digital Processing Board (LDPB) demonstrator: ABBA

- ATCA board : 3 ALTERA FPGAs StratixIV
- Receives up to 320 Super Cell signals from one LTDB
- Waits for TTC trigger to readout Super Cell signals

The role of the ABBA board:

- Receives and decodes the LTDB ADC frames
- Stores these frames
- When a Level-1 Accept (L1A) is received, the correct ADC samples are send out of the board

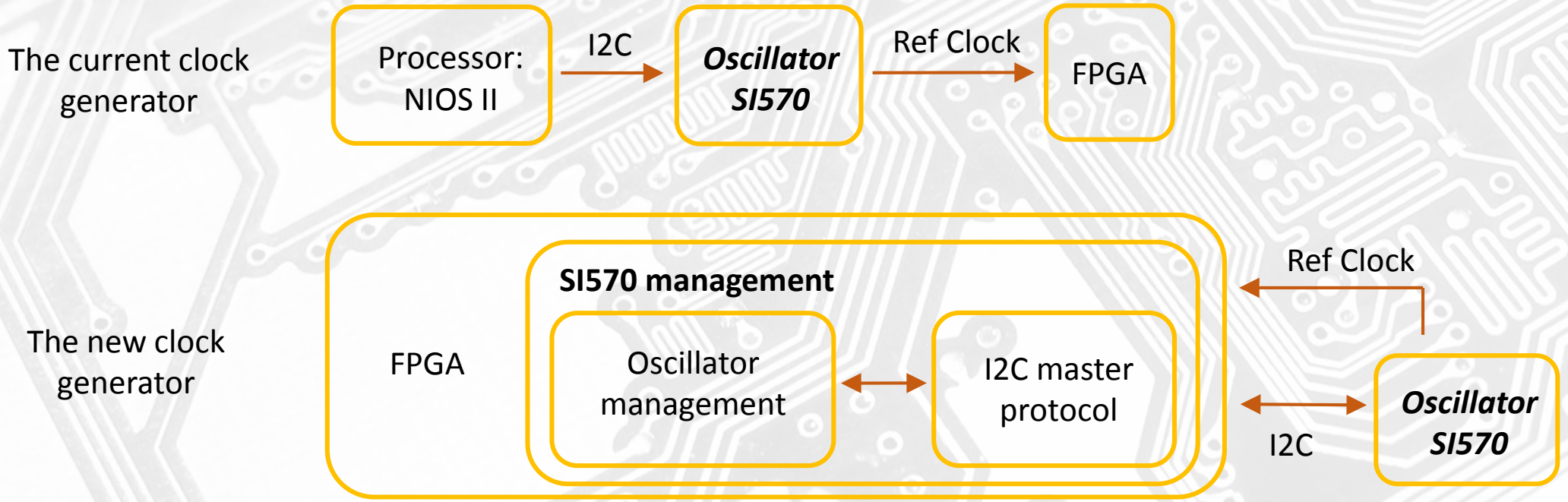


The project on the ABBA board

Presently, the ABBA board clock is generated through an I2C communication from a NIOS II embedded ALTERA processor and a crystal oscillator. The oscillator sends the clock frequency to the FPGA.
Two “loading” steps needed:

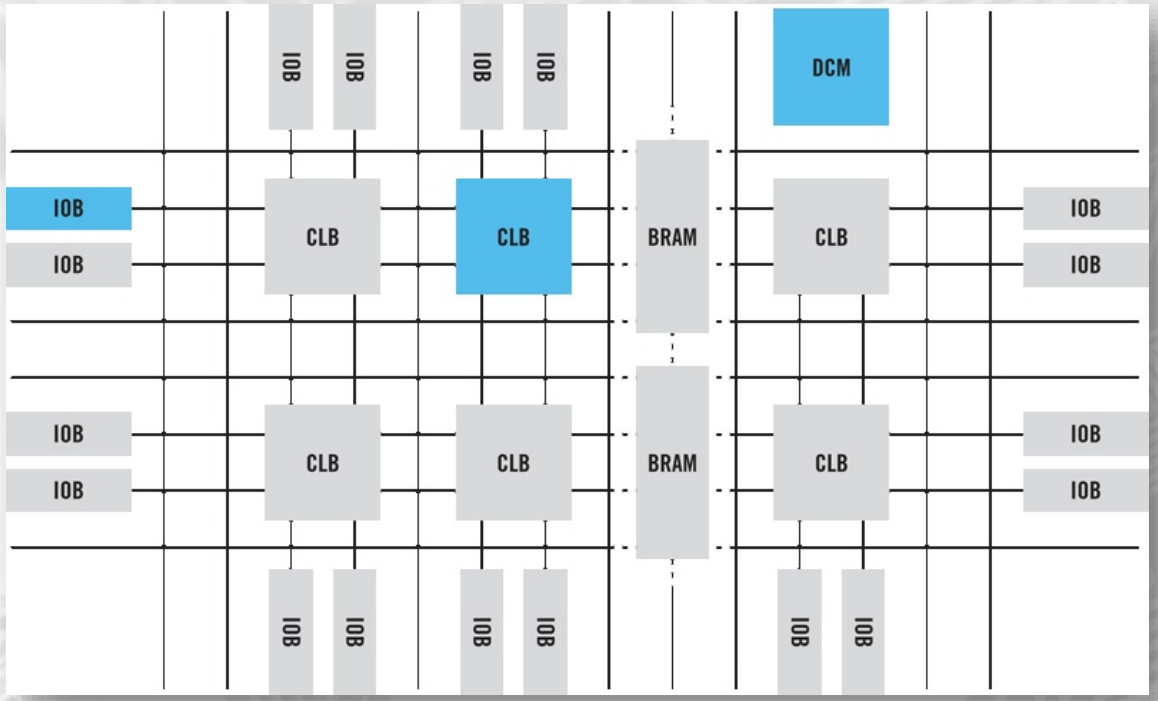
- Processor loading
- FPGA loading

The aim is to have **one loading step**: only the FPGA.



What is an FPGA?

FPGAs are programmable logic devices, made of a matrix of Configurable Logic Blocks (CLBs) connected through programmable interconnections and surrounded by programmable Input/Output Blocks (IOBs).
The FPGA configuration is generally made using an **Hardware Description Language** (HDL).



The use of FPGAs guarantees high computing speed by massive parallel computation and easy reprogrammability as the design evolves.

SI570: the crystal oscillator

A **crystal oscillator** is an electronic oscillator circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a precise frequency.

Si570 Oscillator:

- is programmed via an I2C serial interface
- is user-programmable to any output frequency from 10 MHz to 1.4 GHz
- provides a low-jitter clock with a stable and reliable frequency

In our case:

- frequencies will be 120.24 MHz and 156.25 MHz: the jitter should be about 0.62 ps

The oscillator has been programmed in **VHDL** language (VHSIC Hardware Description Language, where VHSIC is for Very High Speed Integrated Circuits).

The output frequency

The output frequency (f_{out}) generated by oscillator can be obtained starting from this equation:

$$f_{out} = \frac{f_{DCO}}{Output\ Dividers} = \frac{f_{XTAL} \times RFREQ}{HS\_DIV \times N1}$$

Where:

- The internal crystal frequency **f_{XTAL}** is 114.285 MHz
- **RFREQ** is a high-resolution 38-bit multiplier: 10 bit integer part, 28 bit fractional part

HS_DIV × N1 is an integer number that depends on the frequency range:

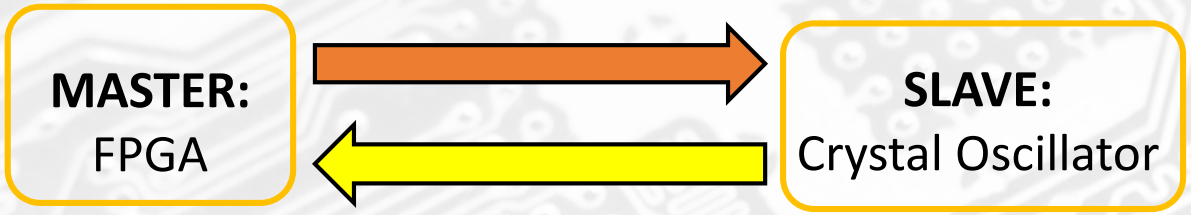
Parameter	Test Conditions	Min	Max	Unit
Output Frequency Range	HS_DIV × N1 > = 6	10	945	MHz
	HS_DIV × N1 = 5 and N1 = 1	970	1134	MHz
	HS_DIV × N1 = 4 and N1 = 1	1.2125	1.4175	GHz

The lowest value of N1 with the highest value of HS_DIV also results in **the best power savings**.

RFREQ, N1 and HS_DIV are the values that will be sent to the oscillator to generate the required frequency.

Sending write command with I2C

The I2C communication is a **master-slave communication**: the FPGA is the master and the crystal oscillator is the slave.



The control interface to the Si570 is an I2C-compatible 2-wire bus for bidirectional communication. The bus consists of a bidirectional **Serial DAta** line (SDA) and a **Serial CLock** input (SCL).

The I2C **SDA write command** is:

S	Slave Address	0	A	Byte Address	A	Data	A	Data	A	…	P

- S – START condition
- 0 – Write command (read command is 1)
- P – STOP condition
- Byte Address – Register address
- Data – Data to be written in the register
- A – Acknowledge (from slave to master)

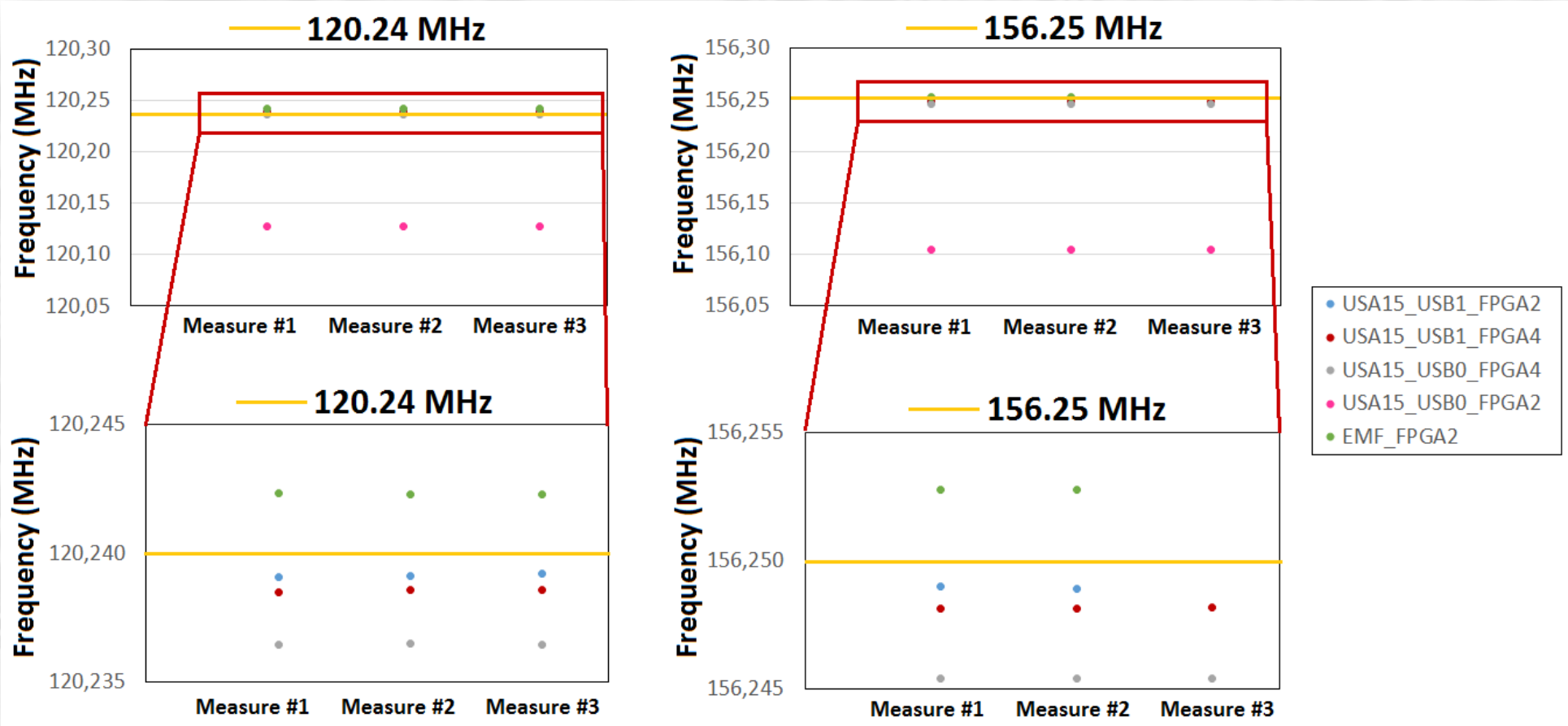
Results

The code has been tested on **three identical ABBA boards**:

- EMF board
- USA15-USB0 board
- USA15-USB1 board

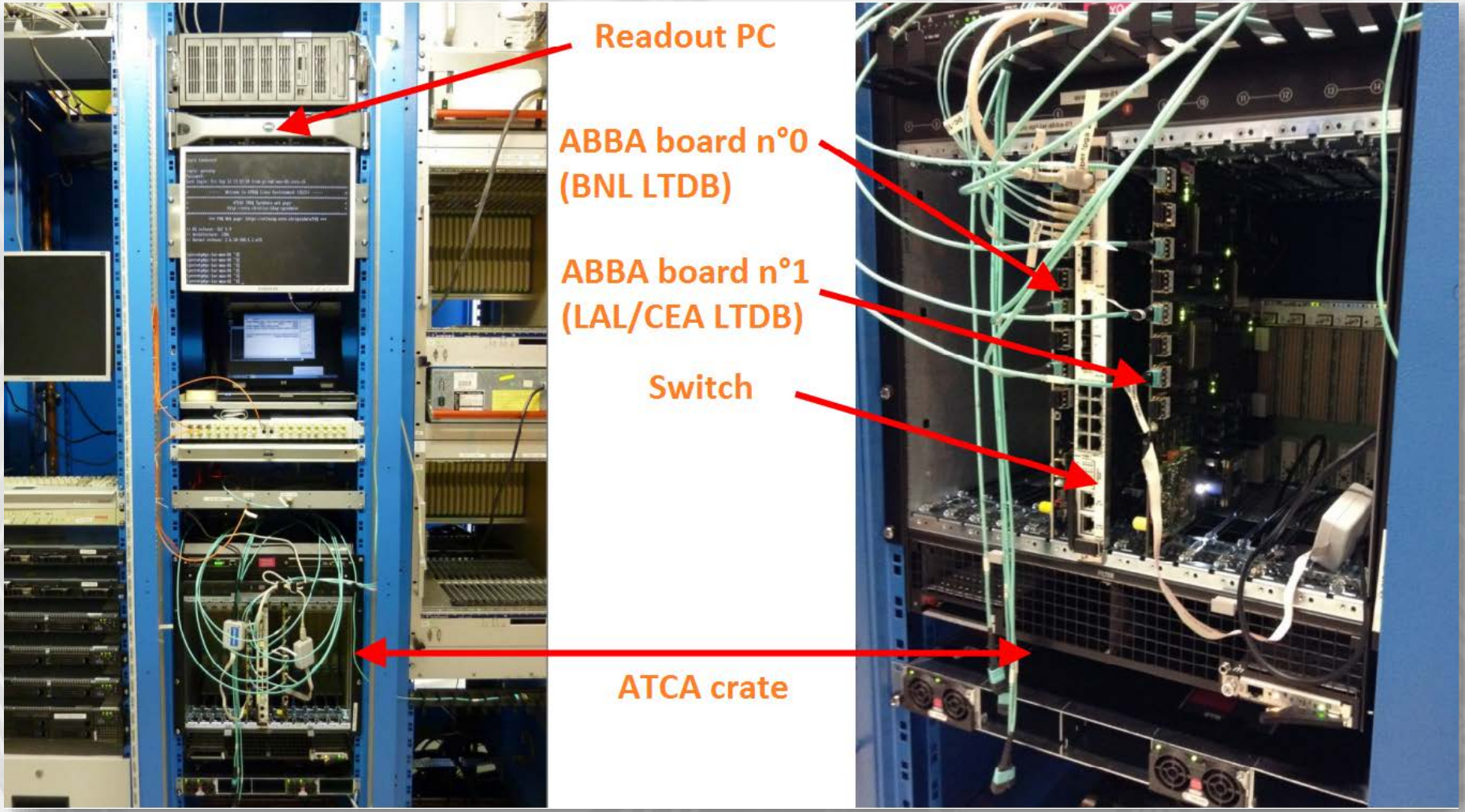
EMF board has only one available FPGA, while USA15 boards have two FPGAs each:
5 FPGAs tested.

There is a systematic error on the FPGA#2 on the USA15-USB0.



The accuracy obtained with the measurements is comparable with the accuracy expected for the crystal oscillator (±2000 ppm).

ABBA demonstrators in ATLAS counting room



In the future

A **new board will substitute the ABBA board.**

An **Advanced Mezzanine Card** (**AMC**) will be built around one Arria 10 Altera FPGA:

- Large capability for internal logic and memory
- Digital Signal Processor (DSP) for signal reconstruction algorithms
- High-speed communications

A **new firmware** is required:
I will implement a VHDL code for the **TTC (Timing, Trigger and Control) distribution** on the FPGA for the new AMC.

What is the TTC?
To maintain coherence inside the experiment it is important to distribute some foundamental information to the readout electronics of all detectors.
The TTC system contains for example the Bunch Crossing (BC) clock, the L1A signal, the EVent IDentifier EVID and the Bunch Crossing IDentifier BCID numbers.

Summary

About ATLAS

- The upgrade of the trigger electronics for the LAr calorimeter will allow a better event selection
- Demonstrator boards have been developed and their perfomances tested

About my project

- The new code for the generation of the clock for the ABBA board is ready
- The data collected with the ABBA board will be soon available to be analysed
- The ABBA board will be substituted by a AMC and a new firmware is required
- I will take part in the development of the firmware

Thank you!

Back up slides

Photons and electrons in the LAr calorimeter

- In the calorimeter, the basic processes for the particles creation are:
  - Figure 1: bremsstrahlung (for electrons)
  - Figure 2: pair production (for photons)
- Electrons and photons interact with the absorber material (lead)
- Secondary particles are created
- When particles have lost sufficient energy, they start to do ionization in the active medium (liquid argon)
- The copper layer collects electrons and a signal is induced on the layer connected to the preamplifier.

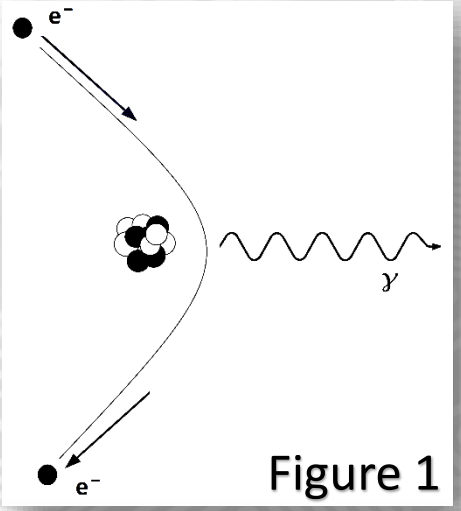
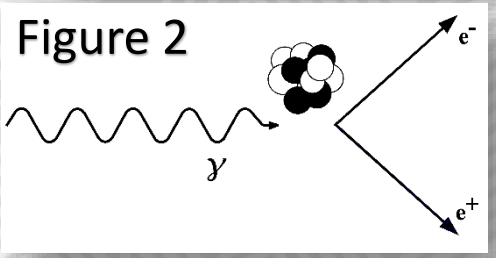
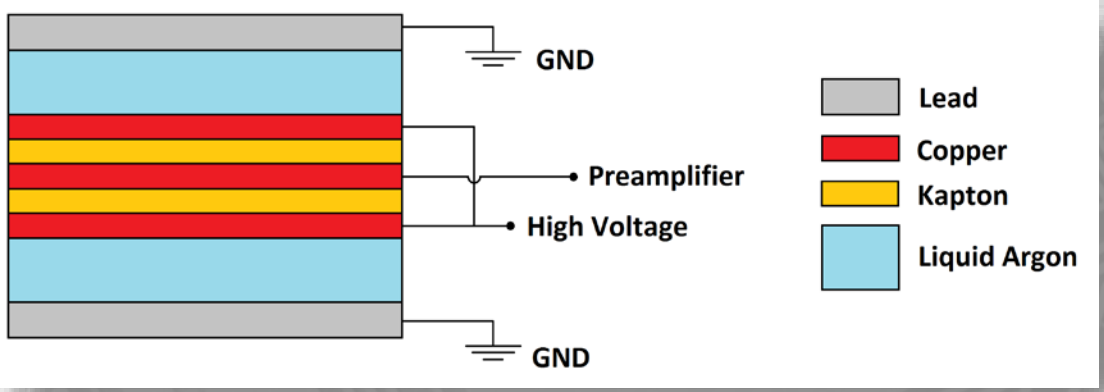
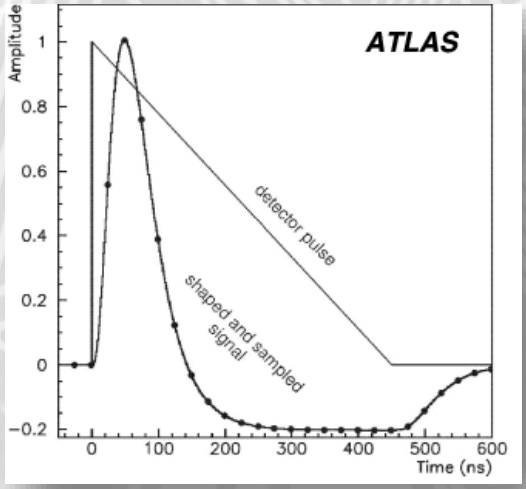


Figure 1

Figure 2







- Accordion geometry: to minimize dead zones.
- Liquid Argon temperature: about 90 °K.

How to obtain the useful values

For 156.25 MHz

The DCO frequency is adjustable in the range of 4.85 to 5.67 GHz.

Starting from $f_{DCO} = f_{XTAL} \times RFREQ$

and nowing that $f_{out} = \frac{f_{XTAL} \times RFREQ}{HS\_DIV \times N1}$ we can obatin $HS\_DIV \times N1 = \frac{f_{DCO}}{f_{out}}$

The range for $HS\_DIV \times N1$ is between 31,04 and 36,288.
The integer value must be choosen between 31 and 36.
In order to have the best power saving I choose $36 = 9 \times 4$.

$$RFREQ = \frac{f_{out} \times HS\_DIV \times N1}{f_{XTAL}}$$

So RFREQ is equal to 49,21905761911 .
Before entering a fractional number into the RFREQ register, it must be converted into a 38-bit binary number:

- The integer portion is converted to a 10-bit binary number
- The fractional portion is multiplied by 2^{28}, truncated and converted to a 28-bit binary number

Finally the two results are concatenated: 0000110001 00111000000101000001010010000.

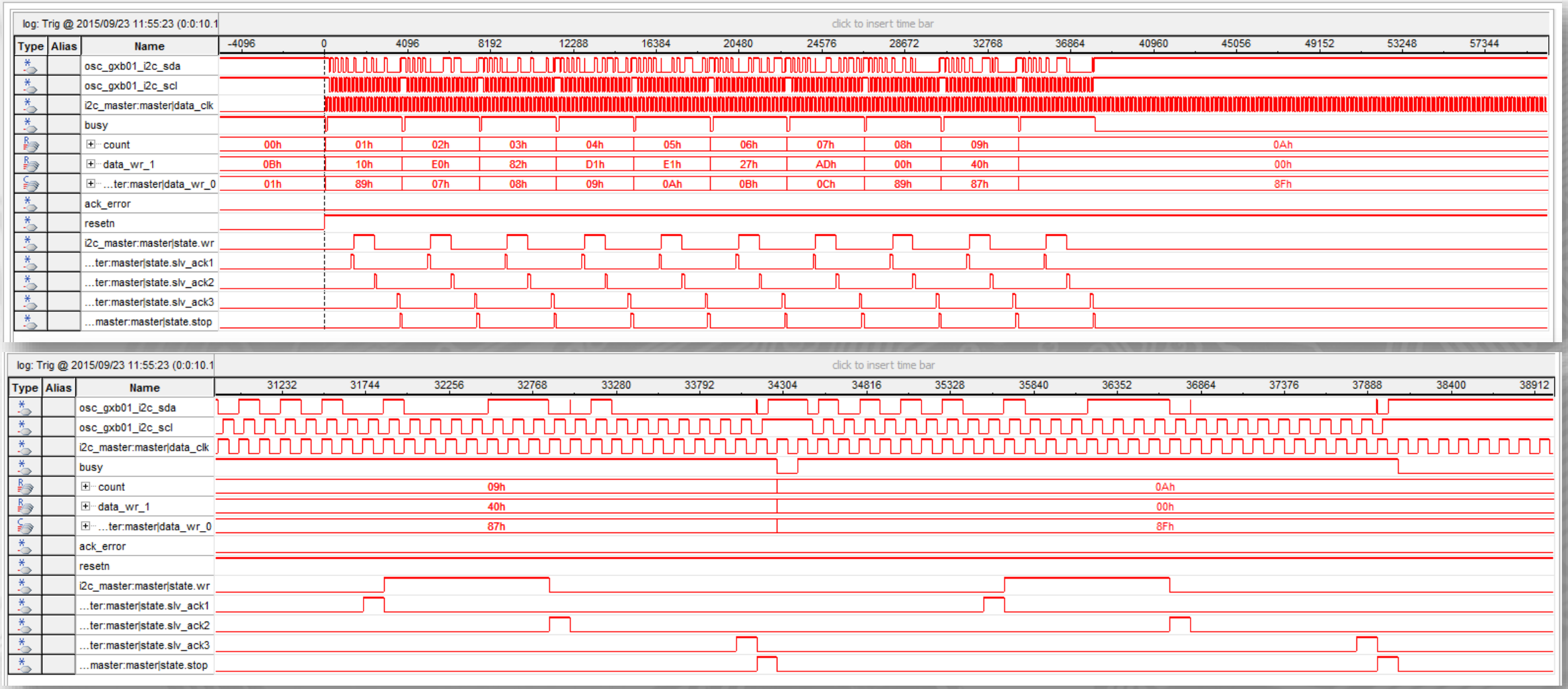
Values to be sent with I2C protocol

120.24 MHz	Decimal	Binary
HS_DIV [3 bit]	11	111
N1 [7 bit]	4	0000011
RFREQ [38 bit]	46,29268932931	00001011100100101011101101101100000001

156.25 MHz	Decimal	Binary
HS_DIV [3 bit]	9	101
N1 [7 bit]	4	0000011
RFREQ [38 bit]	49,21905761911	00001100010011100000010100001010010000

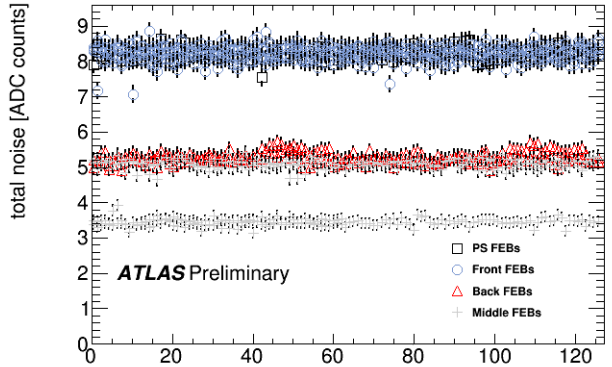
Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7	High Speed/ N1 Dividers	HS_DIV[2:0]			N1[6:2]				
8	Reference Frequency	N1[1:0]			RFREQ[37:32]				
9	Reference Frequency	RFREQ[31:24]							
10	Reference Frequency	RFREQ[23:16]							
11	Reference Frequency	RFREQ[15:8]							
12	Reference Frequency	RFREQ[7:0]							

Looking with the oscilloscope

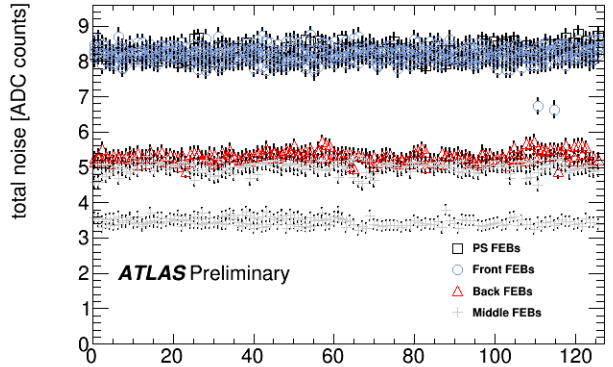


Test on LTDB demonstrator

TOTAL NOISE - The RMS for 128 channels of FEBS in the demonstrator crate installed in ATLAS (left) and a neighbour crate (right) are shown.
The FEBs read out the calorimeter cells.
There are 28 such boards in one Front End Crate (FEC).
The noise levels of the boards vary because different capacitances and gains are applied to their respective cells.



Crate with the demonstrator



Crate without the demonstrator

COHERENT NOISE FRACTION - Here the total noise which is coherent is shown as fraction of the total noise per readout channel (Coherent Noise Fraction = CNF).
The CNF for feedthroughs (FT) 7-12 on the detector has been computed, of which FT 9 and 10 belong to the demonstrator crate.
The board in the first slot reads out the presampler, the boards in the following seven slots read out the front layer, the next two boards the back layer and the last four boards the middle layer of the calorimeter. The last entry is the CNF of the whole halfcrate.