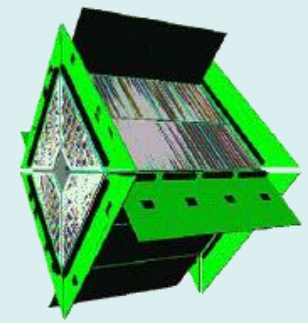




INFN - Milano  
University of Milano  
Department of Physics



# Latest results in ASIC developments for TRACE and other detectors for nuclear physics research

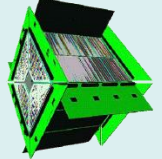
Stefano Capra

"PhD Workshop 2013"

Oct. 14, 2013



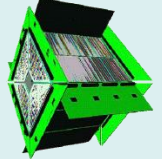
# Outline



- **Context** and **goal of the research**
- **TRACE** detectors & required specs for charge preamps
- From "**Fast - Reset**" preamplifier to "**Fast - Reset**" multichannel
- Non linear **pole - zero** compensation technique
- **Micro - probe** preamplifier: a completely new concept of preamplifier
- **Conclusions**



# Context and goal



## *Context*

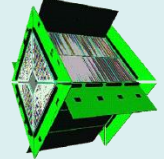
- New generation of nuclear-physics experiments with secondary radioactive beams.
- A technical advance for the FEE applied to the new highly segmentated telescopic silicon detector is required.

## *Goal of the research*

- High-resolution spectroscopy of charged particles implementing a FEE based on a dedicated ASIC multichannel CSP



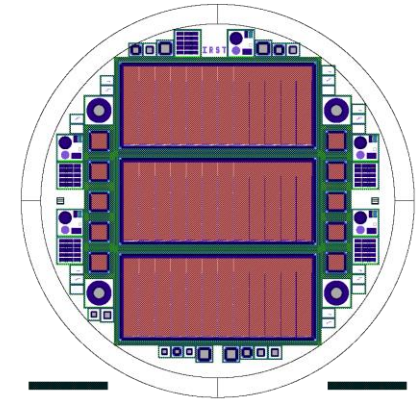
# Highly segmentated Si detectors



High-resolution particle spectroscopy : investigation of nuclear structure approaching the two extreme regions of proton and neutron drip lines

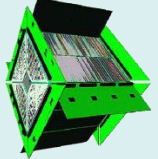
## **Silicon PAD detectors - main features:**

- Operated at **room temperature** (no need for cryogenic temperatures)
- Detector thickness: E pad **1.5mm**,  $\Delta E$  pad **200 $\mu\text{m}$**
- Single pad capacitance value: ~ from **2 pF** to **15 pF**
- Energy dynamics for detected particles: ~ **100 MeV** for  $\alpha$  – particles, **25 MeV** for protons
- Intrinsic energy resolution: **40 keV @ 5.5 MeV** for  $\alpha$  – particles in 200  $\mu\text{m}$  detector
- Segmentation: ~ **4x4 mm** geometry (also 8x8mm)

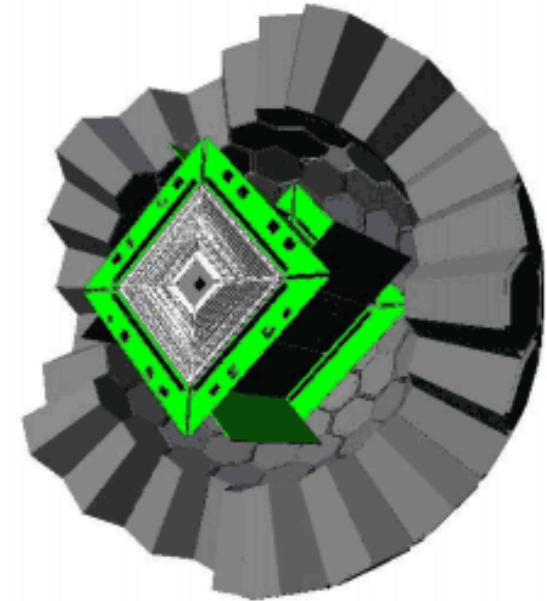




# TRACE detector



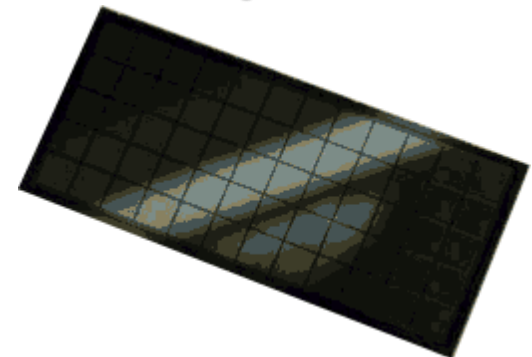
- Fit inside a sphere of 24 cm of diameter
- All the FEE electronics must fit inside the same volume
- Rise time of  $\sim 25$  ns for 200  $\mu\text{m}$  thick  $\Delta E$  layer
- Transparent to  $\gamma$  radiation: coupled with  $\gamma$  spectrometer
- $\sim 10000$  output channels
- $4\pi$  configuration
- 4x4 mm and 8x8 mm segmentation
- Detection of light charged particles, neutron, heavy ions
- Particle discrimination and gamma doppler correction
- Decay spectroscopy



TRACE detector (including electronics) fitting inside AGATA 2n

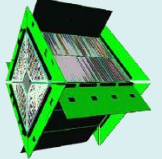
extremely hostile background of highly energetic charge particles in next-generation nuclear physics experiments with high-intensity beams

$\alpha$  ( $\approx 100\text{MeV}$ )  
 $p$  ( $\approx 25\text{MeV}$ )





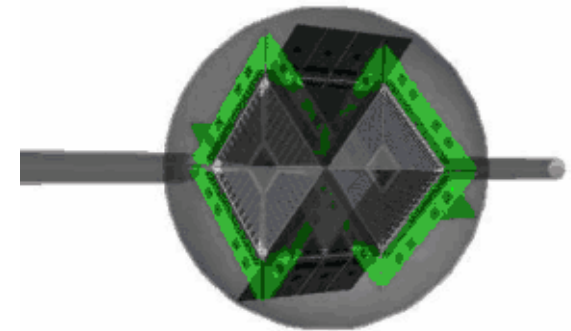
# Charge-preamplifier specifications



- low noise (no more broadening than the intrinsic one)
- Few mW of single - channel power consumption
- excellent stability of the gain and of the shape of the preamplifier response (loop gain  $\sim 10^3$ )
- wide bandwidth: rise time of  $\sim 10$  ns (pulse shape analysis)
- low power consumption (large number of channels operated in vacuum)
- **LARGE DYNAMIC RANGE:**
  - at least  $\sim 10^5$  : from a few keV to 100-200 MeV (or above)
  - minimization of the dead time in a larger energy range up to some hundreds of MeV

extremely hostile background of highly energetic charge particles in next-generation nuclear physics experiments with high-intensity beams

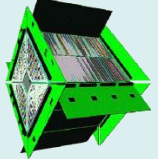
$\alpha$  ( $\approx 100$  MeV)  
 $p$   
( $\approx 25$  MeV)



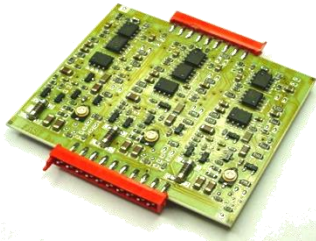
TRACE detector (including electronics) fitting inside a reaction chamber with a radius of 24 cm



# The issue of a wide dynamic range



## Old-style solution: hybrid DISCRETE preamplifiers

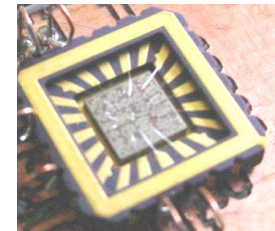


- high flexibility in the design
- use of high voltage power supply (ex: +/- 12 V)
- Absolutely unusable in this context

## Modern CMOS integrated solutions: a mandatory task

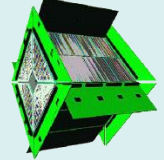
The high segmentation of the detectors yields a higher and higher count of read-out channels (7k – 10k)

- small dimensions (very little space is available for FEE)
- radio-purity
- Low power consumption (operated in vacuum)
- Voltage power supply limited to +/- 2.6 V (limited dynamic range)
- Need for a multichannel ASIC solution





# From "Fast Reset" preamplifier To "Fast Reset Multichannel"

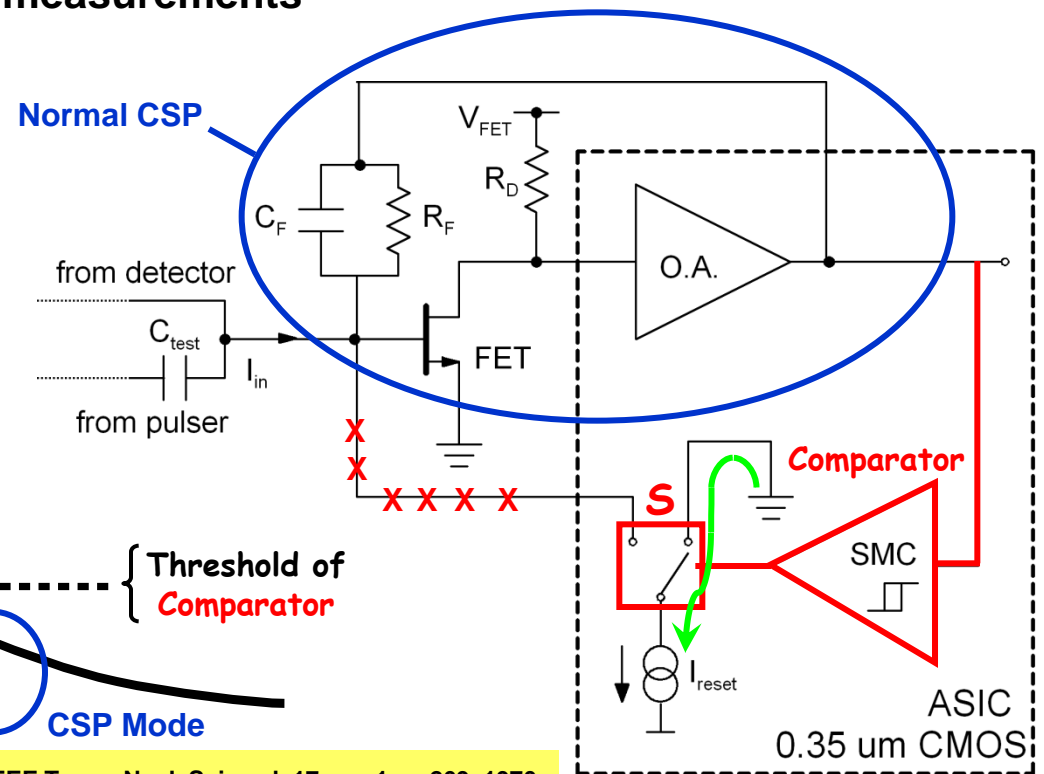
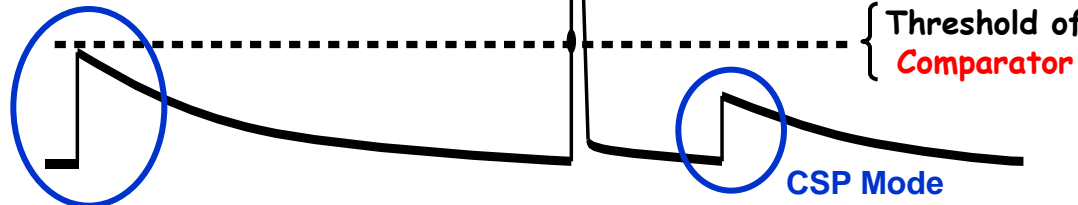


## Charge-Sensitive Preamplifier (CSP) Mode

- For "normal" amplitude signals (up to a few MeV) the **comparator** keeps switch "S" in the right position
- The circuit is a Low-Noise Charge-sensitive preamplifier
- Allows for **high-resolution energy measurements**

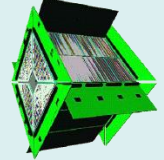
External discrete components:  
 BF862 Si JFET,  $R_F=1G\Omega$ ,  $C_F=1pF$

CSP Mode



\*see also Radeka, Overload Recovery Circuit for Charge Amplifiers, IEEE Trans. Nucl. Sci., vol. 17, no. 1, p. 269, 1970

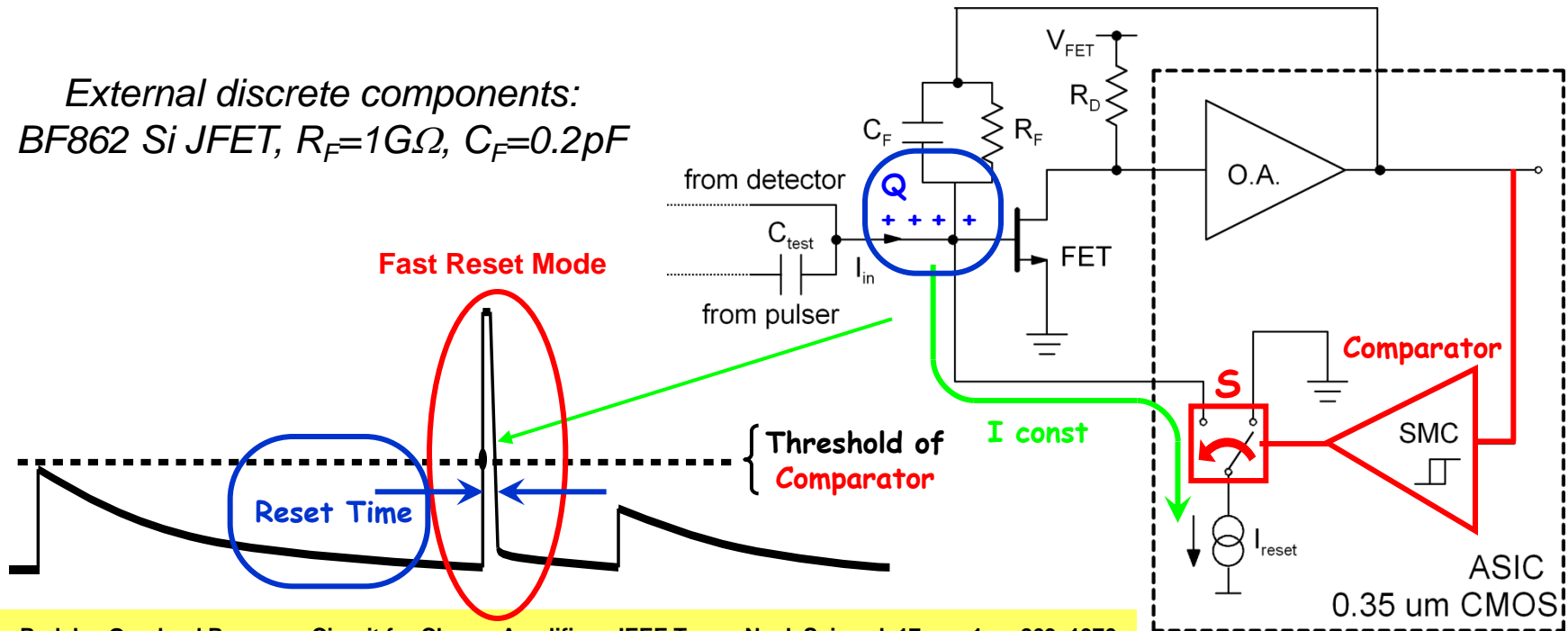




## Fast-Reset Mode

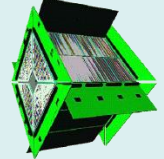
- Minimizes the preamplifier **dead time** and prevents from the paralysis of the acquisition system in the case of extremely high background counting rates
- Allows for **charge information** even in the saturation condition
- Allows for **high-resolution energy measurements** → extending the dynamic range of photons/particles spectroscopy

External discrete components:  
BF862 Si JFET,  $R_F=1G\Omega$ ,  $C_F=0.2pF$



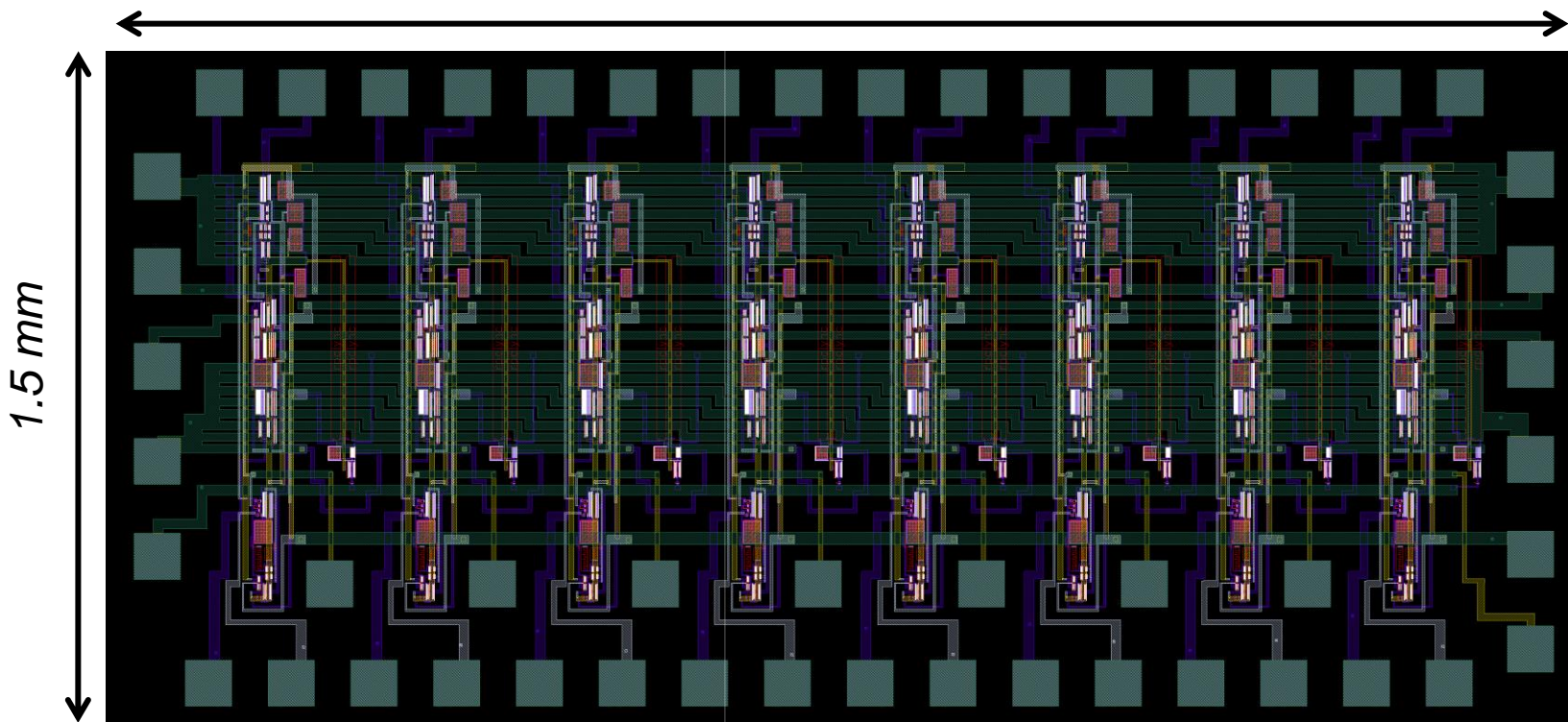
\*see also Radeka, Overload Recovery Circuit for Charge Amplifiers, IEEE Trans. Nucl. Sci., vol. 17, no. 1, p. 269, 1970

# Multichannel device



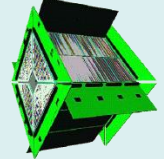
The first realization of the ASIC implements a discrete input stage (BF862) and discrete feedback loop (capacitor and discharge resistance)

3 mm



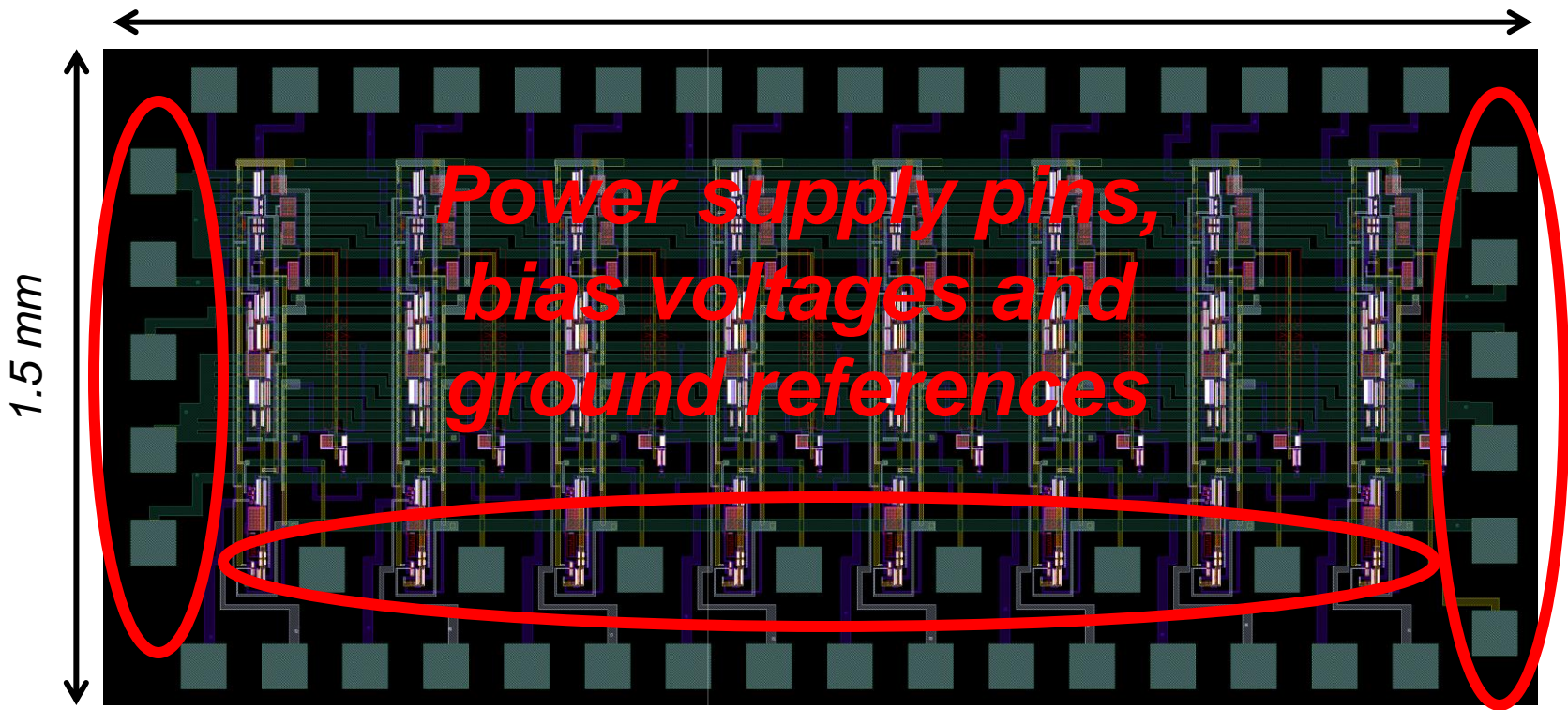
*Layout 0.35µm 5V mid-oxide CMOS*

# Multichannel device



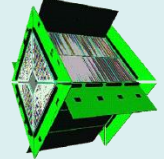
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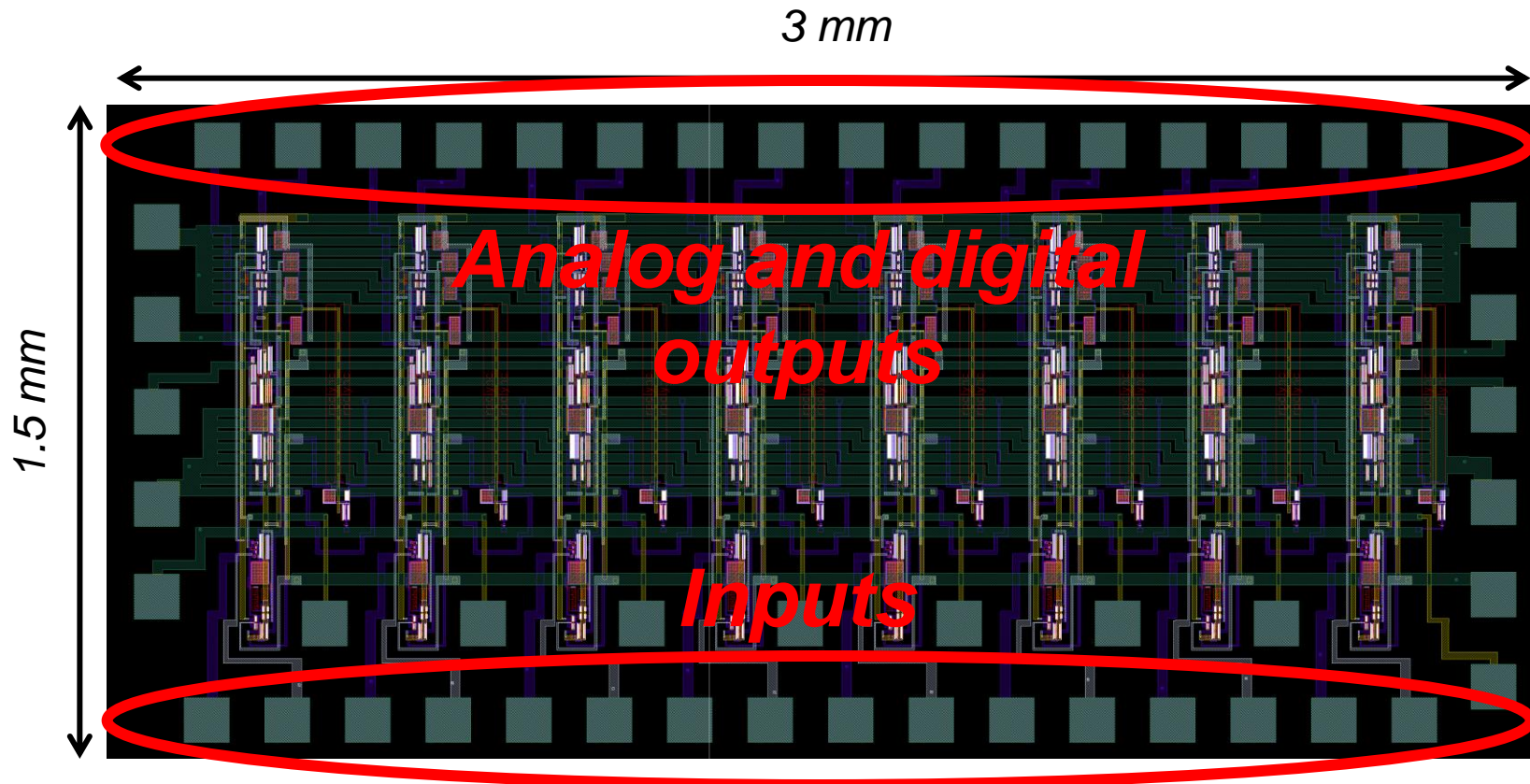


*Layout 0.35 $\mu$ m 5V mid-oxide CMOS*

# Multichannel device



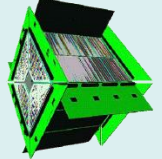
The first realization of the ASIC implements a discrete input stage (BF862) and discrete feedback loop (capacitor and discharge resistance)



*Layout 0.35 $\mu$ m 5V mid-oxide CMOS*



# Integration of the discrete components



In order to provide low ENC the feedback resistance must be as high as possible

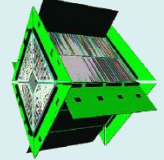
- Common choice for gamma-grade spectroscopy is  $1\text{G}\Omega$
- It would occupy an area of  $2\text{mm}^2$



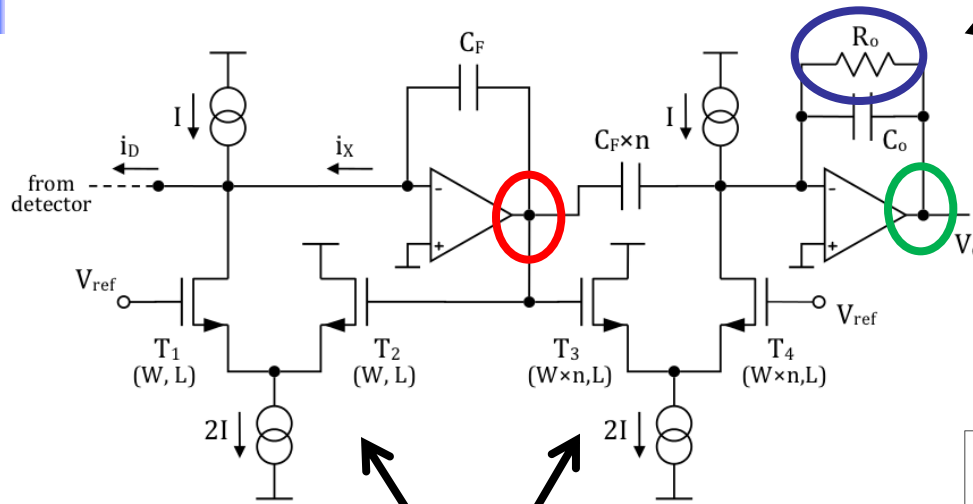
## Common methods for substituting the feedback resistor

- High underthreshold CMOS structure (**NOISE OK** / **LINEARITY PROBLEMS**)
- Linear CMOS transconductor (**LINEARITY OK** / **NOISE PROBLEMS**)

Need for a new structure with provides both linearity and good noise performance, with limited area and power consumption



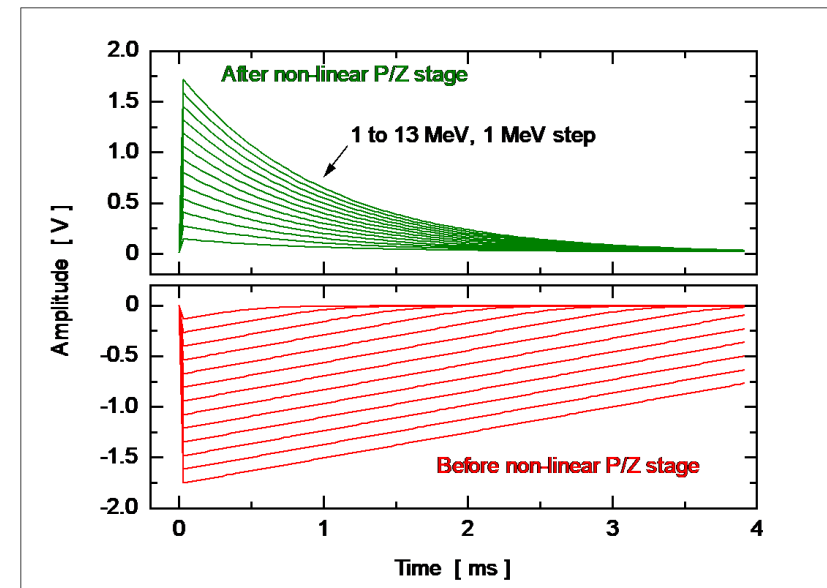
## Concept schematic



10 MΩ resistor

- Reasonable area occupation
- Low capacitive coupling to bulk
- Good noise performance

## Computer simulations

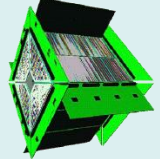


Two transconductors  
with 1:N scale

Clear exponential signal at the output:  
Needed by digital filtering to obtain best  
resolution results



# Microprobe: a completely new concept of preamplifier

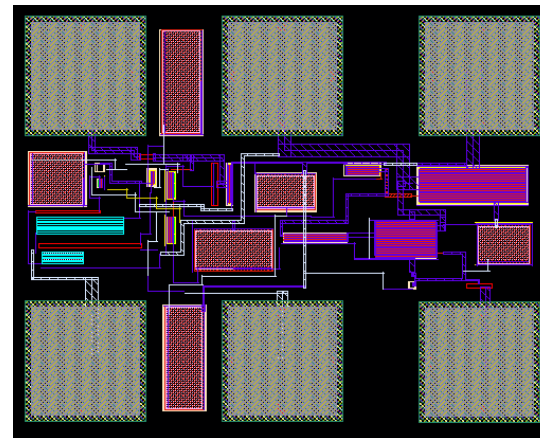
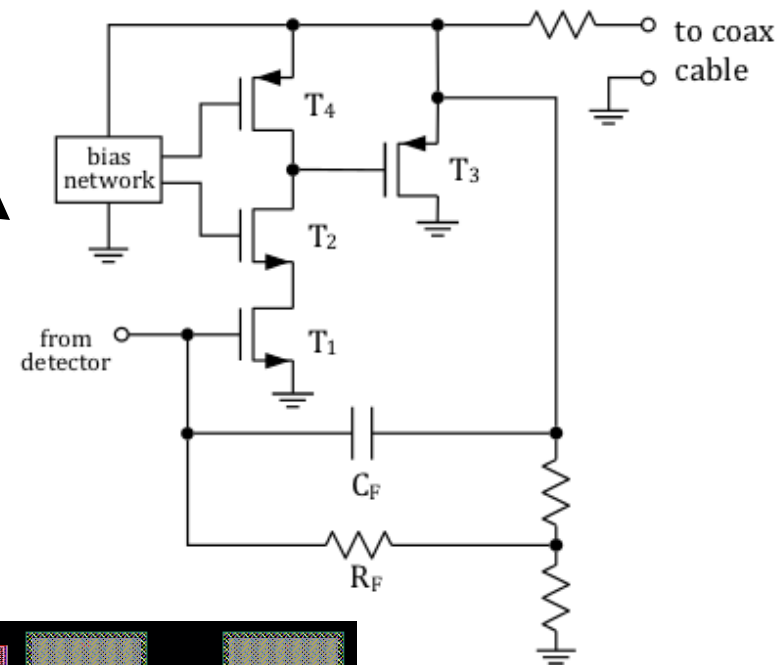


The biasing network: key point of the whole circuit

## Main features

- Only 1 connection with BEE
- No filtering capacitors for power supply
- Signal and power supply on a single node in the circuit
- Drives a  $50\Omega$  cable
- Ultra – fast risetime ( $< 1\text{ ns}$ )
- Good dynamics

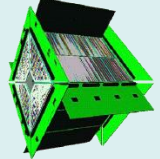
## Concept schematic



Layout in C35B4C3  
Technology  
( $420 \times 330\ \mu\text{m}$ )



# Microprobe: a completely new concept of preamplifier

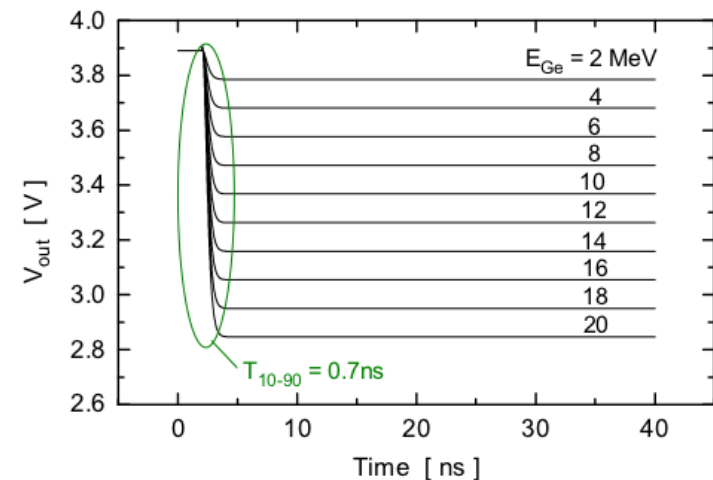
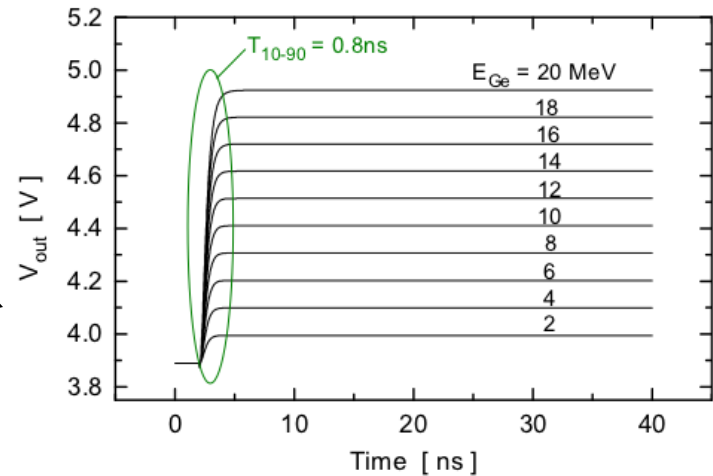


*Both positive and negative dynamics above 20 MeV without appreciable distortion*

## Main features

- *Only 1 connection with BEE*
- *No filtering capacitors for power supply*
- *Signal and power supply on a single node in the circuit*
- *Drives a 50Ω cable*
- *Ultra – fast risetime ( < 1 ns)*
- *Good dynamics and noise performances*

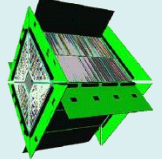
## Computer simulations







# Conclusions



- Design, layout & computer simulation of a JFET-CMOS multichannel preamplifier ( $0.35\mu\text{m}$ ) for Si pad - detectors equipped with a fast reset device for charge sensing stage de-saturation
- Design & computer simulation of the innovative non linear pole – zero compensation technique, which is a great step forward to the total integration of the ASIC CSP.
- Design, layout & simulation of a non – conventional CSP device without power rails and a single power – signal connection to the BEE.
- Layout submission on 21th October 2013: experimental results on realized chips coming soon